REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-36 are pending. Claims 1-36 stand rejected.

Claims 1, 3, 15, 18, 19, 23, 29, 35, and 36 have been amended. Claim 2 has been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 102

Claims 1-3, 10, 11, 13, and 15 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,691,236 of Atkinson ("Atkinson").

Atkinson discloses decreasing the refresh rate of the video graphics controller to a level which allows practical use of the display but consumes much less power than a normal mode. Atkinson discloses using a System Management Interrupt ("SMI") signal and the BIOS to decrease the performance of the video controller, such as to slow the refresh rate and reduce the power of the LCD panel. Atkinson discloses that

> To help assure reliable closing and storage of the computer's state, the innovative method considers whether the battery is at a critically low value, or if a hibernation to disk is occurring (FIG. 2, step 10). In the preferred approach, a Low battery condition is detected by an analog comparator in the interface chip 8 (of FIG. 1) when the main battery charge drops below 10% of maximum charge. The output of the comparator generates a System Management Interrupt (SMI). The SMI interrupts the CPU and executes from System BIOS before returning control of the system to the operating system or application. The BIOS and SMI code will force the video performance to "low."

(Atkinson, col.4, lines 47-58) (emphasis added)

More specifically, Atkinson discloses

> There are 3 elements under software control that control the video performance and refresh rate; the core voltage, VCLK control, and MCLK control. BIOS alone will be allowed to set the performance of the VGC as "low" or normal." Any operating system drivers must make sure that they do not interfere with the operation of BIOS.

> Refresh rate alone is modified by changing the Video clock (VCLK). The performance of the system may be changed through the Memory clock (MCLK).
> The video controller core voltage can also be changed for best power conservation. The core voltage, in the presently preferred embodiment, must be high (5 volts for the 7548 device) when MCLK is at full speed, and is lowered (to 3.3 volts) when video performance is lowered (by lowering the MCLK to below 50 MHz).

(Atkinson, col.9, lines 12-26) (emphasis added)

According to Atkinson, when the BIOS routine has determined that it may enable the low power mode (either low refresh or low performance) it must program the video graphics controller chip (Atkinson, col.9, lines 29-32). In particular, Atkinson discloses

> Four selections of VCLK can be programmed at once in the Cirrus Video controller. Only 1 of these registers is used at one time. The register pairs SR0B and SR1B, SR0C and SR1C, SR0D and SR1D, and SR0E and SR1E determine the four possible VCLK rates. The register MISC (bits 3,2) selects which one of these register pairs will be used to determine the present refresh rate.
> For conventional systems, only 3 of the 4 register sets are necessarily used (for support of 640.times.480, 800.times.600, or 1024.times.768 modes). Registers SR0B/SR1B, SR0C/SR1C, and SR0D/SR1D have been used before for LCD-only, "simulscan" modes (display to an external CRT with the internal LCD enabled), or CRT-only display. For instance, to display an image to the CRT and to the LCD at one time in 640-480 (VGA) mode, set register MISC[3,2] to a 00 so that register pair SR0B/SR1B is used for the VCLK speed. Likewise, register SR0C/SR1C held the correct VCLK when 800.times.600 resolution mode is used, and SR0D/SR1D were used for display of a 1024.times.768 image. No consideration of LCD-only, CRT only, or simultaneous LCD and CRT display has been necessary before to set or select the VCLK given a single resolution mode.
> The preferred embodiment uses the fourth register pair (SR0E/SR1E, with MISC[3,2] set to 1,1) during LCD-only mode. The values of SR0E and SR1E are setup so that the refresh rate is slower than CRT-only refresh could allow (i.e., slower than 45 Hz refresh). For example, display of an 800.times.600 image at 30 Hz refresh implies that the SR0E/SR1E pair is setup for about 20 MHz.
>
> (Atkinson, col.9 line 46 to col.10, line 7) (emphasis added)

Thus, Atkinson discloses that when the BIOS routine upon receiving the SMI signal has determined that it may enable the low power mode, it must program the video graphics controller chip, which has three register pairs storing video clock values corresponding to three particular resolutions of the display, and the fourth register pair to set up the video clock value corresponding to refresh rate during LCD-only mode, which is slower than CRT refresh rate can

allow. Atkinson, unlike the presently claimed matter, does not disclose, teach, or suggest that upon receiving a change indication related to a system power supply, a graphics controller informs a BIOS of a switch in power supply modes, wherein informing includes a request for a set of one or more available clock rates, as recited in amended claim 1:

A method of managing power in a graphics controller, comprising:
Receiving a change indication related to a system power supply;
Adjusting a first clock;
Adjusting a controller power supply voltage; and
Informing a BIOS with an indication of a change related to the system power supply, wherein the informing includes requesting a set of one or more available clock rates.

(Amended claim 1) (emphasis added)

Because Atkinson does not set forth all the limitations of amended claim 1, applicants respectfully submit that amended claim 1 is not anticipated by Atkinson under 35 U.S.C. §102(e).

Given that claims 2-14 depend, directly or indirectly on amended claim 1, and add additional limitations, applicants respectfully submit that claims 2-14 are likewise not anticipated by Atkinson under 35 U.S.C. § 102(e).

Amended claim 15 reads as follows:

A method of effecting power management of a graphics controller in an operating system comprising:
Detecting a change in a system power supply;
Notifying the graphics controller of the change;
Receiving an indication of power reduction in the graphics controller, wherein the receiving the indication includes receiving a request from the graphics controller for a set of available clock frequencies; and
Providing the set of available clock frequencies to the graphics controller.

(Amended claim 15) (emphasis added)

As discussed herein above, Atkinson does not disclose, teach, or suggest the limitation of claim 15 of receiving an indication of power reduction in the graphics controller, wherein the

receiving the indication includes receiving a request from the graphics controller for a set of available clock frequencies.

Therefore applicants respectfully submit that amended claim 15 is not anticipated by Atkinson under 35 U.S.C. § 102(e).

Given that claims 16-22 depend, directly or indirectly on amended claim 15, and add additional limitations, applicants respectfully submit that claims 16-22 are likewise not anticipated by Atkinson under 35 U.S.C. § 102(e).

Rejections Under 35 U.S.C. § 103(a)

Claims 20-22 and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,691,236 of Atkinson ("Atkinson") in view of U.S. Patent No. 5,524,249 of Suboh ("Suboh"). Claims 4, 5, 8, 9, 14 and 23-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6, 691, 236 of Atkinson ("Atkinson"). Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,691,236 of Atkinson ("Atkinson") in view of U.S. Patent No. 6,489,953 of Chen ("Chen"). Claims 6, 7, 16-19, 32 and 33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,691,236 of Atkinson ("Atkinson") in view of U.S. Patent No. 6,618,042 of Powell ("Powell"). Claims 34 and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,691,236 of Atkinson ("Atkinson") in view of U.S. Patent NO. 6,618,042 of Powell ("Powell") as applied to claim 23 above, and further view of U.S. Patent No. 6,489,953 of Chen ("Chen").

As discussed herein above, Atkinson does not disclose, teach, or suggest that upon receiving a change indication related to a system power supply, a graphics controller informs a

BIOS of a switch in power supply modes, wherein informing includes a request for a set of one or more available clock rates, as recited in amended claim 1

Suboh discloses conservation of the power in the video subsystem by inactivating a pixel clock and reducing frequency of a memory clock in response to an indication of user inactivity.

Suboh discloses that

...step of decreasing the memory clock frequency comprises the step of programming a phase lock loop clock circuit to output a clock at a predetermined frequency responsive to a data word from the video controller.

(Suboh, col.9, lines 45-54) (emphasis added)

More specifically, Suboh discloses

FIG. 3 illustrates the communication between the video controller 24 and the PLL 50. The video controller 24 uses two internal PLL serial interface registers, a data register 72 and an Address/Opcode Register 74 to communicate with the PLL 50. Upon writing an address to the Address Register 74, the video controller 24 sets the PLL 50 into serial mode, initiates a MicroWire serial transfer of opcode, address and data to the PLL registers. The PLL registers include two PCLK registers 76 and 78 and two MCLK registers 80 and 82.

(Suboh, col.5, lines 30-40) (emphasis added)

Further, Suboh discloses

When a 0000h is written to the upper and lower PCLK registers 76 and 78, the PLL disables the PCLK signal. When a 0000h is written to the upper and lower MCLK registers 80 and 82, a minimum MCLK signal is output, since MCLK must be enabled in order to refresh the VRAMs 34. In the preferred embodiment, the minimum MCLK is a 1:8 reduction of the normal MCLK frequency.

(Suboh, col.6, lines 27-34) (emphasis added)

Suboh, in contrast to the presently claimed subject matter, discloses that video controller writes into registers of the phase lock loop ("PLL") circuitry to output a clock with a predetermined frequency. Suboh, similarly to Atkinson, does not disclose, teach, or suggest that upon receiving a change indication related to a system power supply, a graphics controller

informs a BIOS of a switch in power supply modes, wherein informing includes a request for a set of one or more available clock rates, as recited in amended claim 1.

Powell discloses a method and apparatus for reducing display brightness on a portable computer when a user switches from an AC adapter to a battery power source. More specifically, Powell discloses

Referring now to FIG. 3B, there is depicted a flow chart illustrating in greater detail the implementation of step 312 of FIG. 3A. When battery use is detected in step 308 (FIG. 3A), the brightness level is then gradually or incrementally reduced according to the rate limiting function in accordance with the present invention in step 316. In step 320, if the target brightness level has not been reached, the process returns to step 316 and the gradual brightness reduction continues. If the target brightness level is reached in step 320, the process continues to step 324 (FIG. 3A).

Referring again to FIG. 3A, after the target brightness level has been set (step 312), the system continues to wait for a change in the power source (step 324). As long as the battery remains in use (step 328), the process returns to step 324 and the display brightness level remains at the target setting (unless it is manually readjusted by the user). If the user then switches from the battery to an external power source, e.g., by reconnecting the AC adapter, the process then returns to step 300 and the brightness level is set to the original user setting.

The rate limiting function may be implemented in a number of ways, for example, (1) by limiting the rate to a maximum incremental brightness decrease per unit time, or (2) by setting a minimum time period, or (3) a fixed time period over which the entire brightness change may occur.

(Powell, col. 5, lines 18-33) (emphasis added)

Thus, Powell merely discloses reducing the brightness of the display according to the rate limiting function and, similarly to Atkinson and Suboh, does not disclose, teach, or suggest that upon receiving a change indication related to a system power supply, a graphics controller informs a BIOS of a switch in power supply modes, wherein informing includes a request for a set of one or more available clock rates, as recited in amended claim 1.

Chen discloses a method and a system for generating CRT ("cathode ray tube") timing signals in a graphic accelerator. More specifically, Chen discloses

Aspects for generating CRT timing signals in a graphics accelerator are described. A method aspect includes shifting reference count values forward by a predetermined count period. A single comparator is utilized to perform a plurality of comparisons between CRT timing signals and at least one of the reference count values during the predetermined count period. Further, compensation for the shifting forward occurs by shifting back signals output from the single

comparator. With the present invention, CRT timing signals are generated through time-shifting of relevant signals. The time-shifting further allows the utilization of a single comparator, which reduces the logic gate requirement and thus the area and cost.

(Chen, Abstract) (emphasis added)

Thus, Chen merely discloses generation of CRT timing signals through time-shifting of relevant signals and similarly to Atkinson, Suboh, and Powel fails to disclose, teach, or suggest that upon receiving a change indication related to a system power supply, a graphics controller informs a BIOS of a switch in power supply modes, wherein informing includes a request for a set of one or more available clock rates, as recited in amended claim 1.

Hence, neither Atkinson, Suboh, Powell, nor Chen discloses, teaches, or suggests that upon receiving a change indication related to a system power supply, a graphics controller informs a BIOS of a switch in power supply modes, wherein informing includes a request for a set of one or more available clock rates, as recited in amended claim 1.

Consequently, even if Atkinson, Suboh, Powell, and Chen were combined, this combination would lack such limitations of amended claim 1.

Therefore, applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. §103(a) over Atkinson, in view of Suboh, and further in view of Powell and Chen.

Given that claims 2-14 depend, directly or indirectly on amended claim 1, and add additional limitations, applicants respectfully submit that claims 2-14 are likewise not obvious under 35 U.S.C. §103(a) over Atkinson, in view of Suboh, and further in view of Powell and Chen.

Because amended claims 15 and 36 contain at least the same limitations as amended claim 1, applicants respectfully submit that amended claims 15 and 36 are likewise not obvious

under 35 U.S.C. §103(a) over Atkinson, in view of Suboh, and further in view of Powell and Chen.

Given that claims 16-22 depend, directly or indirectly on amended claim 15, and add additional limitations, applicants respectfully submit that claims 16-22 are likewise not obvious under 35 U.S.C. §103(a) over Atkinson, in view of Suboh, and further in view of Powell and Chen.

Amended claim 23 reads as follows:

A graphics controller comprising:
A power supply input configured to receive power at a range of voltages from a power regulator;
A power supply control output to provide a trigger signal to the power regulator to change the power supplied to the graphics controller;
A first clock;
And
A system power supply change input.

(Amended claim 23) (emphasis added)

The Examiner noted that Atkinson does not teach a graphics controller having the power supply input being configured to receive power at range of voltages. In fact, Atkinson discloses that

The VGC, in the presently preferred embodiment, may operate at either of 2 voltages, depending on the setting of the PROG pin. The higher voltage may be required for very high refresh rate or memory interface rates are chosen. The PROG pin controls a voltage switch (typically, complementary FETs) so that a "1" on the pin sets the core VCC to 5 volts.

(Atkinson, col.8, lines 19-26) (emphasis added)

Furthermore, Atkinson discloses

Set the core voltage to 3.3 V when MCLK is below 50 MHz and VCLK is set below 77 MHz. The "PROG" pin (an output of the CL-GD7548) is connected to a FET to change the core voltage to the video controller.
Changing from 5 volt operation to 3.3 volt operation (by changing the condition of the PROG pin) saves about 40% of the Video Graphics chip power. For low power mode, set bit 7 of CR30 to "0" for 3.3 V operation of the core.

(Atkinson, col. 10, lines 21-28) (emphasis added)

Thus, Atkinson merely discloses a programmable ("PROG") pin of the video graphics controller chip, which has two descrete ("0" or "1") settings. The "PROG" pin sets the core voltage to one of two predetermined values through FET switch. Atkinson fails to disclose the limitation of amended claim 23 of a power supply input of the graphics controller being configured to receive a power at a range of voltages from a voltage regulator and the power supply control output of the graphics controller that provides a trigger signal to change the power supplied to the graphics controller to enable the graphics controller to regulate, through the trigger signal, the amount of power.

It is respectfully submitted that Atkinson does not disclose, teach or suggest to make the modification of the graphics controller to have a power supply input configured to receive power at a range of voltages from a power regulator and to have a power supply control output to provide a trigger signal to the power regulator to change the power supplied to the graphics controller, as recited in amended claim 23, to enabe the graphics controller to regulate, through the trigger figure, the power. It would be impermissible hindsight, based on applicants' own disclosure, to make such modification on Atkinson's device.

Moreover, even if Atkinson's video graphics controller were modified, as the Examiner suggested, to facilitate selection of a voltage from a range of voltages in order to provide intermediary levels of supply voltage as opposed to two specific voltage levels, such modification would lack the limitations of amended claim 23 of a power supply input of the graphics controller being configured to receive a power at a range of voltages from a voltage regulator and the power supply control output of the graphics controller that provides a trigger signal to change the power supplied to the graphics controller, because the "PROG" pin of the Atkinson's video graphics controller has only two discrete states and, in contrast to the presently

claimed invention, and can not provide continuous control through the trigger signal over the range of the supplied voltages.

Therefore applicants respectfully submit that amended claim 23 is not obvious under 35 U.S.C. §103(a) over Atkinson.

Given that claims 24-34 depend, directly or indirectly on amended claim 34 and add additional limitations, applicants respectfully submit that claims 24-34 are likewise not obvious under 35 U.S.C. §103(a) over Atkinson.

Because amended claim 35 contains at least the same limitations as amended claim 34, applicants respectfully submit that amended claim 35 is likewise not obvious under 35 U.S.C. §103(a) over Atkinson.

In addition, as discussed above, neither Atkinson, Suboh, Powell, nor Chen discloses, teaches, or suggests the limitation of amended claim 23 of a power supply input of the graphics controller being configured to receive a power at a range of voltages from a voltage regulator and the power supply control output of the graphics controller that provides a trigger signal to change the power supplied to the graphics controller.

Consequently, even if Atkinson, Suboh, Powell, and Chen were combined, this combination would lack such limitations of amended claim 23.

Therefore, applicants respectfully submit that amended claim 23 is not obvious under 35 U.S.C. §103(a) in view of the references cited by the Examiner.

Given that claims 24-34 depend, directly or indirectly on amended claim 23, and add additional limitations, applicants respectfully submit that claims 24-34 are likewise not obvious under 35 U.S.C. §103(a) in view of the references cited by the Examiner.

Because amended claim 35 contains at least the same limitations as amended claim 34, applicants respectfully submit that amended claim 35 is likewise not obvious under 35 U.S.C. §103(a) in view of the references cited by the Examiner.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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